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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Takashi KURIHARA, et al.

Application No.: 10/823,649

Group Art Unit: 2825

Confirmation No.: 4917

Filed: April 14, 2004

Examiner: Nghia M. Doan

For: METHOD AND APPARATUS FOR DESIGNING SEMICONDUCTOR INTEGRATED
CIRCUIT

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed May 3, 2006, applicants elect Claims 1-15 and 20-25 of Group I, without traverse.

Respectfully submitted,

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Date:

May 25, 2006

By:

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